Amendments to the Specification:

Please delete the current title beginning at page 1, and replace with the following:

-- Write Queue Descriptor Count Instruction for High Speed Queuing –

Please insert at page 2, line 3 with the following:

-- FIG. 5A is a block diagram of an instruction format. –

Please replace the paragraph beginning at page 3, line 9 with the following amended paragraph:

-- Using a network device 14 implemented as hardware-based 10 multi-threaded processor having multiple microengines 19 ~~(not shown)~~, each CAM entry stores a 32 bit value. Microengines 19 each maintain a plurality of program counters in hardware and states associated with the program counters. Effectively, a corresponding plurality of sets of threads can be simultaneously active on each of the microengines 19 while only one is actually operating at any one time. During a lookup operation CAM entries are compared against a source operand. All entries are compared in parallel, and the result of the lookup is a 6-bit value. The 6-bit result includes a 2-bit code concatenated with a 4-bit entry number. Possible results of the lookup are three fold. A first result is a miss where the lookup value is not in the CAM 28 and the entry number is the Least Recently Used (LRU) entry which can be used as a suggested entry to replace. The second result can be a hit where the lookup value is in the CAM 28 and state bit is clear, and the entry number is an entry which has matched. In addition, a locked result may occur where the lookup value is in the CAM 28, the state bit is set and the 5 entry number is an entry. The state bit is a bit of data associated with the entry, used typically by software. There is no implication of ownership of the entry by any context. --

Please replace the paragraph beginning at page 5, line 8 with the following amended paragraph:

-- Referring to FIG. 3, an example of an output queue 22 and its corresponding queue descriptor 24 is shown. The output queue 22 includes a linked list of elements each of which has a pointer 32 to ~~the~~ a next element's address 34 ~~element 30~~ in the output queue 22. Each element in the linked list 30 includes ~~an~~ the address 34 of information stored in memory 20 that the linked list element represents. The queue descriptor 24 includes a head pointer 36, a tail pointer 38 and a count 40. The head pointer 36 points to the first linked list element 30 of the queue 22, and the tail pointer 38 points to the last linked list element 30 of the output queue 22. The count 40 identifies a number (N) of linked list elements 30 in the output queue 22. --

Please replace the paragraph beginning at page 5, line 20 with the following amended paragraph:

-- Referring to FIG. 4, details of an arrangement of the CAM 28 in a datapath 70 of the network device 14 ~~10 implemented as a processor~~ are shown. A General Purpose Register (GPR) file 72 stores data for processing elements 74. The CAM receives operands as any other processing element 74 would. Operational code (Opcode) bits in an instruction select which processing element 74 is to perform the operation specified by the instruction. In addition, each of the processing elements 74, including the CAM 28, can return a result value from the operation specified by the instruction back to the GPR file 72. –

Please replace the paragraph beginning at page 8, line 1 with the following amended paragraph:

-- The microengine 19 (in ~~a~~ the processor 18 containing multiple microengines 19) tasked with congestion avoidance reads the queue descriptors 24 from memory 20 to determine the length (count word 40) of each output queue 22. The queue descriptors 24 for highly used output queues 22 can remain in the queue array 46 of the memory controller 44 for

an infinitely long time period. A Write_Q_Descriptor_Count Command is issued by the queue manager programming engine 26 after the enqueue or dequeue command, when the entry used "hits" the CAM 28. As shown in FIG. 5A, the format of the command is:

Write _Q Descriptor_Count (address, entry). --

Please delete previous abstract at page 13 and add the following new abstract:

-- Methods and apparatus, including computer program products, for a write queue descriptor count instruction for high speed queuing. A write queue descriptor count command causes a processor to write a single word containing a queue count for each of a plurality of queue entries in a queue array cache. --